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Filing Date	October 22, 2003
First Named Inventor	Han, Dong-Ho
Art Unit	2814
Examiner Name	Le, Thao X.
Attorney Docket Number	P16829

ENCLOSURES *(Check all that apply)*

- [ ] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment / Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
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- [ ] Information Disclosure Statement
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Date	December 5, 2006	Reg. No.	34,860

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Signature			
Typed or printed name	Edith Martin	Date	December 5, 2006

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant: HAN et al.

Application Serial No.: 10/690,928

Filing Date: October 22, 2003

For: DIFFERENTIAL SIGNAL TRACES COUPLED WITH HIGH PERMITTIVITY MATERIAL

Confirmation No.: 6901

Group Art Unit: 2814

Examiner: Thao X. Le

APPEAL BRIEF

Attorney Docket No.: P16829

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Dated: December 5, 2006 By: Edith Martin

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner in the Final Office Action mailed August 21, 2006 (the "Final Office Action"), rejecting claims 6, 7, 29-32 and 36-38.

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REAL PARTY IN INTEREST

The present application is assigned to INTEL CORPORATION, 2200 Mission College Blvd., Santa Clara, California 95052.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to Appellants, Appellants' legal representative, or assignee, which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 6, 7, 29-32 and 36-38 are pending and stand rejected.

Claims 1-5, 8-28 and 33-35 have been cancelled.

STATUS OF AMENDMENTS

No amendments were filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is concerned with printed circuit boards (PCBs) on which a pair of signal traces is formed for differential signaling. (Specification, page 2, lines 3-4)

Substrates for PCBs may be constructed of an inhomogeneous material in which fibers are embedded in resin. (Specification, page 2, lines 4-6) The inhomogeneity of the PCB substrate may interfere with proper differential signaling via a pair of traces on the substrate. That is, if one trace of the pair of traces passes over a fiber in the substrate, and the other trace does not, then common mode noise may result. (Specification, page 2, lines 6-10)

For this and other reasons, the present inventors have recognized that it is desirable to improve the coupling between the two traces of a pair of traces provided for differential

signaling. In particular, the present application teaches that the space between the two signal traces may be filled with a high permittivity material having a higher dielectric constant than the dielectric constant of the resin in the PCB substrate. (Specification, page 4, lines 16-23; FIG. 1: filler material 44 between signal traces 42; filler material 32 between signal traces 30.) As a result, the performance of the signal trace pair may be improved and/or trace density may be increased. (Specification, page 4, lines 23-29)

* * * * * * *

Appellants will now map the limitations of the independent claims to the relevant portions of the disclosure.

Claim 6

"a substrate"--dielectric layer 34 (FIG. 1); specification, page 4, lines 3-8.

"a pair of signal traces formed directly on the substrate and spaced from each other"--signal traces 42 (FIG. 1); specification, page 4, lines 5-8.

"a filler material directly on the substrate and between the signal traces, the filler material having a dielectric constant that is higher than a dielectric constant of a material of which the substrate is formed"--filler material 44 (FIG. 1); specification, page 4, lines 8-10 and lines 17-19.

"a solder mask layer directly on the signal traces and directly on the filler material, the dielectric constant of the filler material being higher than a dielectric constant of the solder mask layer"--solder mask layer 46 (FIG. 1); specification, page 4, lines 13-15 and 19-21.

"the filler material has a height that is substantially equal to a height of the signal traces" --specification, page 7, lines 3-5.

Claim 31

"a substrate"--dielectric layer 34 (FIG. 1); specification, page 4, lines 3-8.

"a pair of signal traces formed on the substrate and spaced from each other"--signal traces 42 (FIG. 1); specification, page 4, lines 5-8.

"a filler material on the substrate and between the signal traces, the filler material having a dielectric constant that is higher than a dielectric constant of a material of which the substrate is formed"--filler material 44 (FIG. 1); specification, page 4, lines 8-10 and lines 17-19.

"a metal ground plane on an opposite side of the substrate from the signal traces"--ground plane 26 (FIG. 1); specification, page 3, line 18.

"the filler material has a height that is substantially equal to a height of the signal traces" --specification, page 7, lines 3-5.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 6, 7, 29-32 and 36-38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Asai et al. (hereinafter "Asai"), U.S. Patent No. 6,392,898, in view of either Behling et al. (hereinafter "Behling"), U.S. Patent No. 6,373,719 or Brandt et al. (hereinafter "Brandt"), U.S. Patent No. 6,068,782.

ARGUMENT

I. Applicable law

The law governing application of 35 U.S.C. § 103(a) is set forth in general terms as follows in *In re Kotzab*, 217 F.3d 1365 (Fed.Cir. 2000):

> A claimed invention is unpatentable if the differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art [citing § 103(a)].

In comparing the claimed invention with the prior art, both the claimed subject matter as a whole and the prior art as a whole must be considered. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143 (Fed.Cir. 1985). The invention as a whole includes "not only ... the subject matter which is literally recited in the claim in question ... but also ... those properties of the subject matter which are inherent in the subject matter *and* are disclosed in the specification." *In re Antonie*, 559 F.2d 618, 620 (CCPA 1977), [emphasis in original].

During examination before the PTO, claim terms are given their broadest reasonable interpretation, consistent with the specification (*In re Hyatt*, 211 F.3d 1367, 1372 (Fed.Cir. 2000); i.e., claim terms are given their plain meaning unless defined to the contrary in the specification (*In re Zletz*, 893 F.2d 319, 321 (Fed.Cir. 1989)). The plain meaning of a term is the

meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed.Cir. 2005).

Furthermore, a *prima facie* finding of obviousness cannot properly be made unless all the limitations of the claimed invention are taught or suggested by the prior art. *In re Royka*, 490 F. 2d 981 (CCPA 1974).

II. Overview of Prior Art Relied upon by the Examiner

To aid this honorable Board in considering the relevant prior art as a whole in connection with the claims at issue, appellants will now summarize the most pertinent teachings of the references relied upon by the Examiner.

A. Asai

The Asai reference is primarily concerned with preventing warping of a "package board" on which an integrated circuit (IC) is to be mounted.[1] Asai accomplishes this objective by adding electronically non-functional "dummy" metallization regions on the side of the package board substrate that has the smaller quantity of electrically functional metallization.[2]

According to the portion of Asai apparently deemed most pertinent by the Examiner, the package board of Asai has a resin filler 40 present between portions of metal layer 34U (from which signal lines 58U are formed) on core board 30.[3] The Examiner apparently concedes that Asai does not teach or suggest that the filler 40 have a dielectric constant higher than the core board 30.

B. Behling

The Behling reference is primarily concerned with providing an IC package which protects the IC mounted thereon from excessive transient voltage levels.[4] Behling proposes to

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[1] Column 3, lines 46-62.

[2] Dummy pattern 58M, FIG.2; column 6, line 48 to column 7, line 4; column 3, lines 53-62.

[3] FIG. 4(E); column 8, lines 57-61; signal lines 58U seen in FIG. 2 and discussed at column 6, lines 14-18 and column 6, line 62 to column 7, line 1.

[4] Column 3, lines 1-3; column 4, lines 31-43.

achieve this goal be filling a microgap 38 between a contact portion 34 and a ground bar 36 with a "variable voltage material" 40.[5] During normal voltage conditions, the variable voltage material 40 electrically isolates the ground bar 36 from the contact portion 34. However, in the event of a high voltage transient, the variable voltage material converts to a low resistance, allowing current to be channeled from the contact portion to ground, thereby protecting the IC.[6]

Evidently the variable voltage material 40 may have a high dielectric constant.[7]

C. Brandt

The Brandt reference discloses a technique for forming embedded capacitors in PCBs.

The portions of Brandt's disclosure that the Examiner cites[8] refer to (a) a capacitor dielectric;[9] (b) a low dielectric constant insulator 120[10] which the Examiner refers to as a "filler"[11], and which in fact is patterned by photo-masking so as to define the location in which the capacitor dielectric is to be deposited[12]; and (c) an element 190 (FIG. 6), which the Examiner refers to as a "signal line"[13], and which the reference itself refers to as an "electrical via"[14].

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[5] Column 4, lines 31-35.

[6] Column 4, lines 35-43.

[7] Column 5, line 38 to column 6, line 60.

[8] In a rather inconsistent and puzzling manner, in appellants' view.

[9] Reference numeral 130 in FIG. 4 and reference numeral 180 in FIG. 5, and discussed at column 3, lines 26-29 and 63-65 and column 4, lines 18-41.

[10] FIG. 1; discussed at column 2, lines 19-24 and 39 and column 4, lines 10-17.

[11] Final Office Action, page 4, line 13.

[12] Brandt, column 2, lines 21-24 and 65-67; column 3, lines 19-28.

[13] Final Office Action, page 4, line 14.

[14] Brandt, column 2, line 53.

III. Claims 6, 7, 29-32 and 36-38 are patentable over both of the combinations of references proposed by the Examiner

Appellants' primary contentions in connection with this appeal can be summarized as follows: The Asai reference, upon which the Examiner primarily relies, arguably teaches a pair of signal traces having a resin filler in between. The present application claims a filler between two signal traces where the filler has a dielectric constant higher than the dielectric constant of a material in the substrate on which the traces are formed. There is no teaching in the secondary references (Behling or Brandt) that would lead one of ordinary skill in the art to modify Asai's structure so as to substitute a high dielectric constant material for the resin filler.

Claim 6 is taken as exemplary of all of the pending claims for the purposes of this argument.

The Examiner concedes[15], half-heartedly but correctly, that Asai does not disclose a filler, between two signal traces, that has a higher dielectric constant than a material used in the substrate upon which the two signal traces are formed. The question to be resolved in regard to this, appellants' main argument, is whether this defect of Asai is compensated for by the teachings of either Behling or Brandt. Appellants believe the answer is that they clearly do not.

Behling teaches that a variable voltage material 40, having a high dielectric constant, is to be filled in between a contact portion 34 and a ground bar 36. The purpose of the variable voltage material is to isolate the ground bar 36 from the contact portion 34 during normal operation, and to channel current from the contact portion to the ground bar if a high transient voltage occurs.[16]

The Examiner's reliance on this disclosure is misplaced. The prior art discloses no reason to channel current from one of Asai's signal lines to another of Asai's signal lines. It is only necessary to insulate one signal line from the other, and this is done adequately by Asai's resin filler. There is no need to replace Asai's resin filler with a filler having a higher dielectric constant than the substrate.

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[15] Final Office Action, page 3, lines 4-7.

[16] Behling, column 4, lines 31-43.

The function served by Behling's high-dielectric constant filler is to protect a neighboring IC by providing a path to ground for excessive current. Since neither signal line in Asai is a ground, channeling current from one signal line to the other would not provide protection to Asai's IC, nor would it serve any other useful purpose taught or suggested by the prior art. Behling's teachings regarding a high dielectric filler between a contact and ground has no relevance to Asai's neighboring signal lines, and does not support the Examiner's proposal to modify Asai's structure by replacing Asai's resin filler with a filler having a high dielectric constant.

For these reasons, considering the invention claimed in claim 6 as a whole and the proposed combination of Asai and Behling as a whole, the claimed invention is not obvious, because the two references, considered together, would not lead one of ordinary skill in the art to modify Asai's structure in the manner proposed by the Examiner. Neither of the two references discloses any reason, motivation or problem that would suggest that there was a need for or benefit from modifying Asai's structure by changing the resin filler to a high dielectric material.

The Brandt reference is equally insufficient to support the Examiner's proposed modification of Asai's structure. The Brandt reference merely discloses use of a high dielectric constant material between the plates of a capacitor formed from metal layers embedded in a PCB. One of ordinary skill in the art would have no reason to replace Asai's resin filler between two signal lines with a capacitor dielectric. Asai's neighboring signal lines are not capacitor plates, and the prior art does not suggest any benefit to be gained by increasing the capacitance between Asai's neighboring signal lines.

It is therefore appellant's position that all of the pending claims are nonobvious in view of their recitation of a filler, between paired signal traces, and having a higher dielectric constant than a material used in the substrate on which the traces are formed.[17]

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[17] Appellants will also take this opportunity to contest the Examiner's proposed interpretation of "signal traces" as encompassing any "electrically conductive material". (Final Office Action, page 7, lines 8-9) Such an overly expansive and unreasonably broad interpretation runs contrary to the holdings of *Zletz* and *Phillips*, *supra*, to the effect that claim terms are to be given their plain meaning, as understood by those who are skilled in the art. Those who are skilled in PCB design would understand a "signal trace" not only as limited to a conductive element, but also further limited to elements that are configured and positioned to carry signals along a horizontal dimension or dimensions of a PCB from one part of the PCB to another. Accordingly, those skilled in the art would consider a "signal trace" to be distinct from other conductive elements, such as capacitor plates, ground bars, contacts, vias, etc.

IV. Additional argument in support of patentability of claims 6, 7, 29, 30, 36-38.

Claim 6 is taken as exemplary of the group of claims covered by this additional argument.

Principally in this regard, appellants wish to point out that the element 44 of Asai, apparently considered by the Examiner to be a "solder mask layer,"[18] in fact is no such thing. Referring to column 9, line 55 to column 10, line 42 of Asai, it appears that the layer 44 is merely a "resin insulation material" (column 9, lines 55-57). Subsequent steps on layer 44 include photo-masking, etching and electroless plating. Nowhere is it stated or suggested in the reference that layer 44 has a solder masking or solder resist function. It is only a subsequent layer--70 in FIG. 9(U)--that is described as a "solder resist layer" (column 11, lines 38-51). Of course, layer 70 is not "directly on the signal traces [metal regions 34U in Asai]" nor "directly on the filler material [element 40 in Asai]", and so fails to satisfy the corresponding limitations of claim 6 in regard to the recited "solder mask layer".

It follows that the "all elements" rule of *Royka*, *supra*, is not satisfied by the Examiner's proposed combination of references, and that claims 6, 7, 29, 30 and 36-38 are patentable on this additional basis.

[18] Final Office Action, page 3, line 1.

CONCLUSION

The rejection appealed from is improper at least because the references relied upon by the Examiner, considered as a whole, fail to teach or suggest the claimed invention. Therefore, Appellants respectfully request that the Examiner's rejections be reversed.

This Brief is filed within two months from the date of mailing of the Notice of Appeal (*i.e.*, within two months of October 10, 2006); as such, no extension of time is believed due. However, if any additional fees are due in conjunction with this matter, the Commissioner is hereby authorized to charge them to Deposit Account 50-1852. An Appendix of claims involved in this appeal is attached hereto.

If any issues remain, or if the Examiner or the Board has any further suggestions for expediting allowance of the present application, kindly contact the undersigned using the information provided below.

Respectfully submitted,

December 5, 2006
Date

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Attachment: Appendix of claims

APPENDIX A--CLAIMS

1-5. (canceled)

6. An apparatus comprising:

a substrate;

a pair of signal traces formed directly on the substrate and spaced from each other;

a filler material directly on the substrate and between the signal traces, the filler material having a dielectric constant that is higher than a dielectric constant of a material of which the substrate is formed; and

a solder mask layer directly on the signal traces and directly on the filler material, the dielectric constant of the filler material being higher than a dielectric constant of the solder mask layer;

wherein the filler material has a height that is substantially equal to a height of the signal traces.

7. The apparatus of claim 6, wherein the filler material has a dielectric constant in excess of 4.

8-28. (canceled)

29. The apparatus of claim 6, wherein the filler material includes polyvinylidene diflouride.

30. The apparatus of claim 6, further comprising:

a metal ground plane on an opposite side of the substrate from the signal traces.

31. An apparatus comprising:

a substrate;

a pair of signal traces formed on the substrate and spaced from each other;

a filler material on the substrate and between the signal traces, the filler material having a dielectric constant that is higher than a dielectric constant of a material of which the substrate is formed; and

a metal ground plane on an opposite side of the substrate from the signal traces;

wherein the filler material has a height that is substantially equal to a height of the signal traces.

32. The apparatus of claim 31, wherein:

the signal traces are formed directly on the substrate;

the filler material is directly in contact with the substrate; and

the ground plane is directly in contact with the substrate.

33-35. (canceled)

36. The apparatus of claim 6, wherein the substrate includes a resin in which fibers are embedded, the dielectric constant of the filler material being higher than a dielectric constant of the resin.

37. The apparatus of claim 6, wherein the signal traces are formed of copper.

38. The apparatus of claim 6, wherein the filler material substantially fills a space between the signal traces.

APPENDIX B - EVIDENCE

No evidence is being submitted with this Appeal Brief (*i.e.*, this appendix is empty).

APPENDIX C - RELATED PROCEEDINGS

No prior or pending appeals, interferences, or judicial proceedings are known to Applicants, Applicants' legal representative, or assignee, which may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal. Therefore, there are no copies of decisions rendered by a court or the Board to attach (*i.e.*, this appendix is empty).